**DIGITAL LOGIC DESIGN**

**LAB -12**

**SEQUENTIAL CIRCUITS DESIGN**

**Objective:** Student should understand how to design a sequential circuit given its specifications in sentence structure or state diagram or state table form.

**Analyze the given sequential circuit. Fill the table given below and mention the following:**

1. Input equations
2. Output equations
3. Excitation equations
4. Next state equations
5. State diagram
6. Q
7. R

D Q

R

A

B

Q0

Q1

Z

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Current States** | | **Inputs** | | **Next States** | | **Output** |
| **Q0** | **Q1** | **A** | **B** | **Q0 (t+1)** | **Q1**  **(t+1)** | **Z** |
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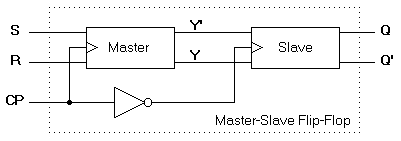
**Lab Task 1:**

**Implement the SR Master-Slave flip flop on logic works. Also, show the timing diagram.**

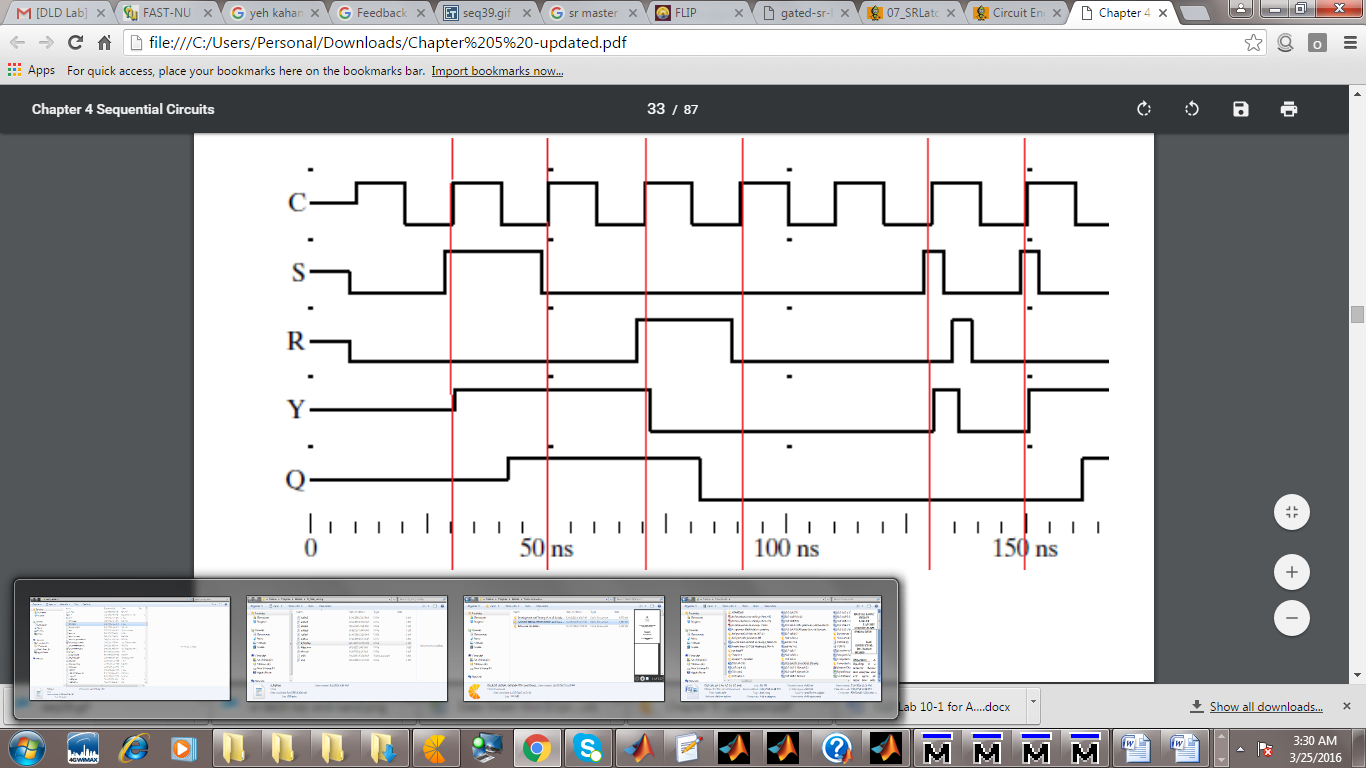
***Note:***

* *Draw the Combinational Circuit diagram using NAND & NOT gates.*
* *For clock pulse (CP) use “clock” component available in Logic works.*
* *Label the diagram properly*

**Logic Diagram:**



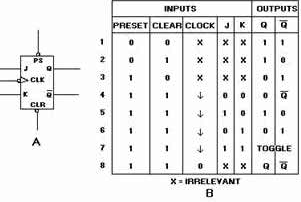
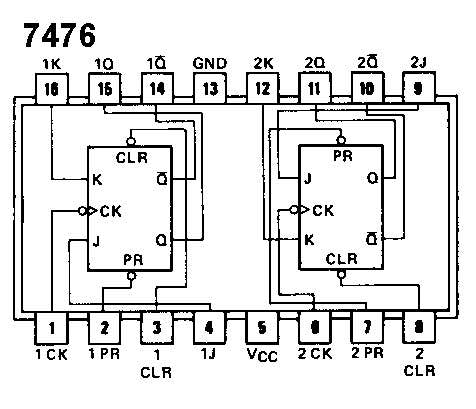
**Timing Diagram:**

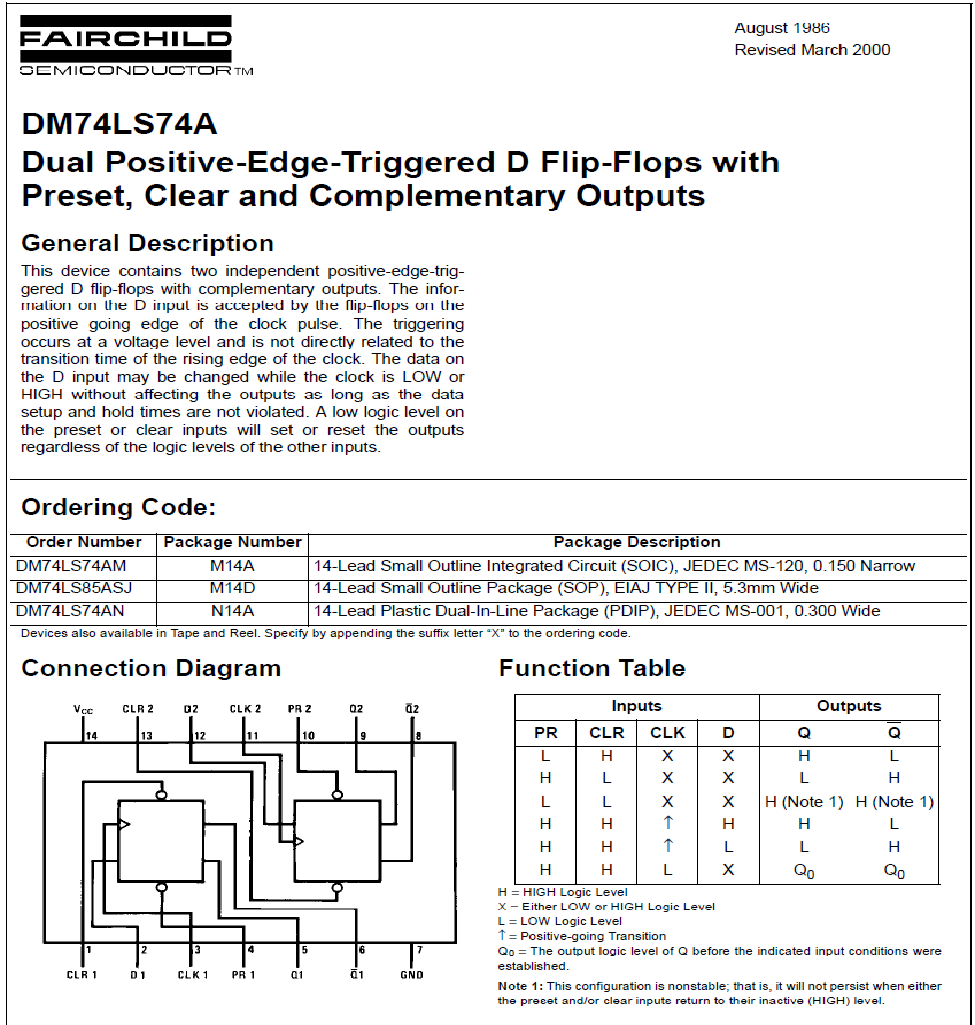


**Lab Task 2:** Perform on Logic Works and test the ICs of D-Flip flop & JK flip flop so that is fulfils their tables (get familiar with inputs & outputs)

**Lab Task 3:**

Perform on Logic Works by using IC of JK-Flip flop and construct master-slave flip flop using JK FF IC.

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